09/971,958

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	457	1 adj shaped adj (spacer or sidewall or (side adj wall))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 09:17	
2	BRS	L2	320791	257/$.ccls. or 438/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 09:20	
3	BRS	L3	77	1 and 2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:57	
4	IS&R	L4	1065	((438/303) or (438/304)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:45	

	Error Definition	Errors
1		0
2		0
3		0
4		0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	IS&R	L5	2273	((257/288) or (257/344) or (257/346) or (257/389)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:47	
6	BRS	L6	218	double adj spacer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:58	
7	BRS	L7	31	6 same thickness	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 15:59	

	Error Definition	Errors
5		0
6		0
7		0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	457	1 adj shaped adj (spacer or sidewall or (side adj wall))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 09:17	
2	BRS	L2	320791	257/$.ccls. or 438/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 09:20	
3	BRS	L3	77	1 and 2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 13:57	
4	IS&R	L4	1065	((438/303) or (438/304)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:45	

	Error Definition	Errors
1		0
2		0
3		0
4		0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	IS&R	L5	2273	((257/288) or (257/344) or (257/346) or (257/389)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/07/25 14:47	

	Error Definition	Errors
5		0

DERWENT-ACC-NO: 2003-446659

DERWENT-WEEK: 200342

TITLE: Semiconductor device production, having different size of gate spacer, comprises use of double-spacer structure to control spacer thickness of internal gate device and peripheral gate device

INVENTOR: CHEN, H; HOU, J ; LIN, K ; LIN, T ; TSAI, J

PATENT-ASSIGNEE: UNITED MICROELECTRONICS CORP[UNMIN]

PRIORITY-DATA: 1999TW-0103442 (March 5, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 502375 A	September 11, 2002	N/A	000	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
TW 502375A	N/A	1999TW-0103442	March 5, 1999

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: TW 502375A

BASIC-ABSTRACT:

NOVELTY - The production of small-sized gate structure containing a double-layer spacer structure comprises providing a gate oxide layer on a semiconductor substrate surface and forming a polysilicon layer on top of the gate oxide layer.

DETAILED DESCRIPTION - A conducting layer is formed on the polysilicon layer and is followed by forming a first dielectric layer on top of the conducting layer. A first photoresist layer is formed on top of the first dielectric layer and is followed by using an anisotropic etching manner to etch the photoresist layer, part of the first dielectric layer, the conducting layer, the polysilicon layer and the gate oxide layer to form an internal gate device and the peripheral gate device. A second dielectric layer is formed on the periphery of the internal gate device and the peripheral device. A

third dielectric layer is formed on top of the second dielectric layer, and a fourth dielectric layer is formed on top of the third dielectric layer. A photoresist layer is formed on the fourth dielectric layer of the internal gate device and anisotropic etching is used to etch the fourth dielectric layer of the peripheral gate device to form a second spacer of the peripheral gate device. Anisotropic etching is used to etch the third dielectric layer of the peripheral gate device to form a first spacer of the peripheral gate device. The photoresist layer of the internal gate device and the fourth dielectric layer are removed. A fifth dielectric layer is formed on top of the third dielectric layer of the internal gate device. The fourth dielectric layer of the peripheral gate device and the second dielectric layer on top of the gate device surface are removed. The fifth dielectric layer is formed on the first dielectric layer and the third dielectric layer of the peripheral gate device, and a photoresist layer is formed on top of the fifth dielectric layer. Finally, anisotropic etching is used to etch the photoresist layer, the internal gate device for having semiconductor substrate bit line contact window, and the peripheral gate device for having gate bit line contact window as well as semiconductor substrate bit line contact window.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: SEMICONDUCTOR DEVICE PRODUCE SIZE GATE SPACE COMPRISE DOUBLE SPACE STRUCTURE CONTROL SPACE THICK INTERNAL GATE DEVICE PERIPHERAL GATE DEVICE

DERWENT-CLASS: L03 U11

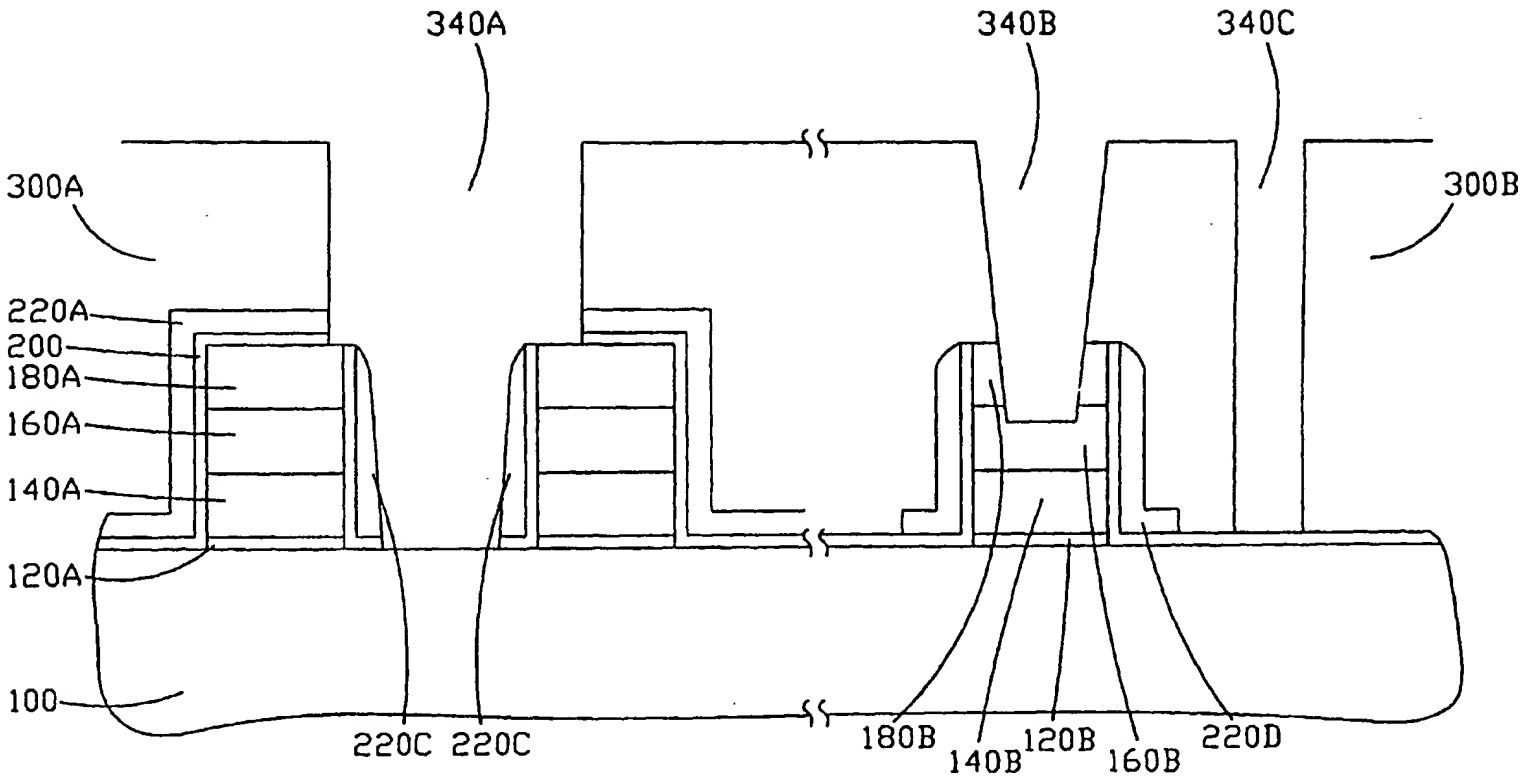
CPI-CODES: L04-C07; L04-C10; L04-C10B; L04-C12A;

EPI-CODES: U11-C05D; U11-C05F1;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2003-118633

Non-CPI Secondary Accession Numbers: N2003-356100


340A
340B
340C
300A
300B
220A
200
180A
160A
140A
120A
100
220C
220C
180B
140B
120B
160B
220D